REMARKS

The following remarks are responsive to the August 18, 2004 Office Action. Claims 1, 6-8, and 10-18 remain as previously presented and Claims 2-5 and 9 remain as originally filed. Thus, Claims 1-18 are presented for further consideration. Please reconsider the claims in view of the following remarks.

Response to Rejection of Claims 1, 3, and 10-12 Under 35 U.S.C. § 103(a)

In the August 18, 2004 Office Action, the Examiner rejects Claims 1, 3, and 10-12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,502,161 issued to Perego et al. ("Perego").

Claim 1

Claim 1 recites (emphasis added):

> 1. A memory module comprising:
> a printed circuit board;
> a plurality of identical integrated circuits mounted in at least two rows onto at least one surface of the printed circuit board;
> a control logic bus connected to the plurality of identical integrated circuits; and
> a first register and a second register connected to the control logic bus, the first register addressing the identical integrated circuits located in a first row and a second row of identical integrated circuits on a first lateral portion of the at least one surface of the printed circuit board, and the second register addressing the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral portion of the at least one surface of the printed circuit board.

At paragraph [0035], the present application describes an embodiment of the invention recited by Claim 1 as follows:

> the address signals to the integrated circuits 102 in the top and bottom row ... on one half of the memory module 100 are routed from a common register 302 via a set 303 of signal paths. The address signals to the integrated circuits 102 on the second half of the memory module 100 ... are routed from a common register 304 via a second set 305 of signal paths. The use of the bilateral symmetry allows closer matching of timing performance for the signals from the integrated circuits 102, improves the timing performance, and provides greater performance timing margins than traditional design guidelines in which each integrated circuit in a row of integrated circuits 102 is connected to a single register.

Thus, certain embodiments of the invention recited by Claim 1 use the configuration of having the memory devices on one lateral portion of the memory module connected to a first register and the memory devices on a second lateral portion of the memory module connected to a second

register to advantageously provide improved timing performance as compared to prior art memory modules with only a single register. Therefore, Applicants submit that the two-register structure recited by Claim 1 provides benefits not taught or suggested by the prior art.

In contrast, Perego discloses a memory system which utilizes memory modules each having a single buffer device connected by a point-to-point architecture to the rest of the memory system. Perego does not teach or suggest a memory module having "a first register and a second register" as recited by Claim 1. In addition, Perego does not teach or suggest having "the first register addressing the identical integrated circuits located in a first row and a second row of identical integrated circuits on a first lateral portion of the at least one surface of the printed circuit board," or having "the second register addressing the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral portion of the at least one surface of the printed circuit board," as recited by Claim 1 (emphasis added).

The Examiner states that the invention recited by Claim 1 can be viewed as slight modifications from design preferences from the disclosure of Perego. The Examiner further states that it would have been obvious to implement the two registers as recited by Claim 1 as opposed to a single buffer chip. However, because the invention recited by Claim 1 provides benefits not taught or suggested by the prior art, as discussed above, Applicants submit that the invention recited by Claim 1 is more than a slight modification from design preferences. Rather, the invention recited by Claim 1 is a significant departure from routine design preferences, and represents a novel and non-obvious system for improving the performance of a memory module. Applicants submit that Claim 1 is patentably distinguished from Perego.

Furthermore, Perego teaches away from using more than one buffer device per memory module. As disclosed by Perego at column 6, lines 57-59, using a single buffer device (emphasis added) "effectively reduces the number of loading permutations on the corresponding point-to-point link to one, thus simplifying test procedures."

Perego further discloses using a single buffer device no matter how many memory devices are on the memory module. For example, Perego discloses at column 9, lines 1-28 and Figures 3B and 4B that memory modules with more memory devices can be achieved by using a single buffer device and increasing the number of channels, even with double-sided memory modules. In this way, Perego teaches away from using more than one buffer device per memory module.

Applicants submit that, contrary to the Examiner's assertion, it would not be obvious to persons skilled in the art to vary the design disclosed by Perego to make a memory module with a two-register structure recited by Claim 1. Pursuant to M.P.E.P. § 2141 (Rev. 2, May 2004), to reject a claim under 35 U.S.C. § 103(a), the cited prior art references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination. In particular, pursuant to M.P.E.P. § 2141.03 (emphasis in original), "a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." Because Perego teaches away from the design variation being asserted by the Examiner to reject Claim 1, Applicants submit that Claim 1 is patentably distinguished over Perego. In addition, because the two-register structure recited by Claim 1 provides benefits not taught or suggested by the prior art, as discussed above, Applicants submit that Claim 1 is patentably distinguished over Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claim 1 and pass Claim 1 to allowance.

Claims 3, 10, and 11

Each of Claims 3, 10, and 11 depend from Claim 1, so each of Claims 3, 10, and 11 includes all the limitations of Claim 1, as well as other limitations of particular utility. Therefore, Applicants submit that Claims 3, 10, and 11 are patentably distinguished from Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claims 3, 10, and 11 and pass these claims to allowance.

Claim 12

Claim 12 recites:

> A memory module comprising:
> a printed circuit board;
> a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;
> a control logic bus connected to the plurality of identical integrated circuits; and
> a first register and a second register connected to the control logic bus, the first register addressing the identical integrated circuits located in the first row and the second row of identical integrated circuits on a first lateral portion of the at least one surface of the printed circuit board, and the second register addressing the identical integrated circuits located in the first row and the second row of identical integrated circuits on a second lateral portion of the at least one surface of the printed circuit board.

For the reasons discussed above in relation to Claim 1, Applicants submit that Claim 12 is patentably distinguished over Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claim 12 and pass Claim 12 to allowance.

Response to Rejection of Claims 2, 4, and 5 Under 35 U.S.C. § 103(a)

In the August 18, 2004 Office Action, the Examiner rejects Claims 2, 4, and 5 under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of U.S. Patent No. 6,705,877 issued to Li et al. ("Li"). The Examiner states that Perego did not clearly disclose all the limitations of Claims 2-5 and that Li discloses these limitations. The Examiner further states that it would be obvious to modify the system disclosed by Perego to include the features of Li.

As discussed above, Perego does not teach or suggest all the limitations of Claim 1. Applicants submit that Li does not teach or suggest the limitations of Claim 1 which are not disclosed by Perego and that it is not obvious to combine the disclosures of Perego and Li. Therefore, Applicants submit that Claim 1 is patentably distinguished over the combination of Perego and Li.

Each of Claims 2, 4, and 5 depends from Claim 1, so each of Claims 2, 4, and 5 includes all the limitations of Claim 1, as well as other limitations of particular utility. Therefore, Applicants submit that Claims 2, 4, and 5 are patentably distinguished from Perego in view of Li. Applicants respectfully request that the Examiner withdraw the rejection of Claims 2, 4, and 5 and pass these claims to allowance.

Response to Rejection of Claims 6-9 and 13-18 Under 35 U.S.C. § 103(a)

In the August 18, 2004 Office Action, the Examiner rejects Claims 6-9 and 13-18 under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of U.S. Patent No. 6,594,167 issued to Yamasaki et al. ("Yamasaki").

As discussed above, Perego does not teach or suggest all the limitations of Claim 1. Applicants submit that Yamasaki does not teach or suggest the limitations of Claim 1 which are not disclosed by Perego and that it is not obvious to combine the disclosures of Perego and Yamasaki. Therefore, Applicants submit that Claim 1 is patentably distinguished over the combination of Perego and Yamasaki. Similarly, Applicants submit that Claim 12 is patentably distinguished over the combination of Perego and Yamasaki.

Each of Claims 6 and 8 depends from Claim 1, Claim 7 depends from Claim 6, and Claim 9 depends from Claim 8. Each of Claims 6-9 therefore includes all the limitations of

Claim 1, as well as other limitations of particular utility. Each of Claims 13-15 and 17 depends from Claim 12, Claim 16 depends from Claim 15, and Claim 18 depends from Claim 17. Each of Claims 13-18 therefore includes all the limitations of Claim 12, as well as other limitations of particular utility. Therefore, Applicants submit that Claims 6-9 and 13-18 are patentably distinguished from Perego in view of Yamasaki. Applicants respectfully request that the Examiner withdraw the rejection of Claims 6-9 and 13-18 and pass these claims to allowance.

Summary

For the foregoing reasons, Applicants submit that Claims 1-18 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 10/27/04 By: _____

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